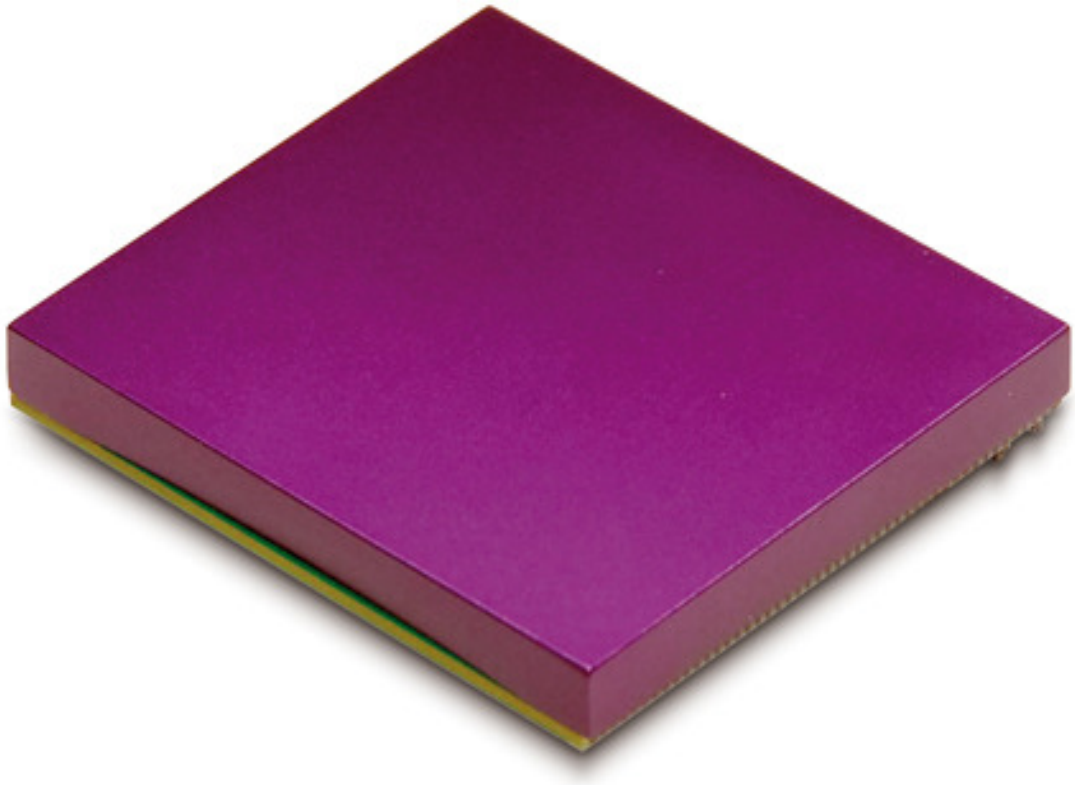
DIGITAL-LOGIC
smart embedded computers

TECHNICAL USER MANUAL FOR:

smartCore *Express* SMA200



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CE

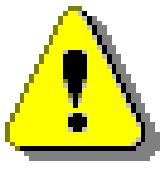
For internal use only:
File: SMA200_TechManual_V1.0.doc
Path: R:\HANDBUCH\smart\SMA200\SMA200_TechManual_V1.0.doc

About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V0.1	07.2008 KUF	Initial Version
V1.0	***09.2008 WAS***	***Details fine-tuned / Standard format w/Eng. applied***



Attention!
1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

Table of Contents

1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. DIGITAL-LOGIC AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, DIGITAL-LOGIC AG does not accept any liability arising from the use or application of any circuit or product described herein.

1.1. Trademarks

DIGITAL-LOGIC, DIGITAL-LOGIC-Logo, MICROSPACE, and smartModule are registered trademarks owned worldwide by DIGITAL-LOGIC AG, Luterbach (Switzerland). In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

1.2. Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. DIGITAL-LOGIC AG shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

1.6. Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support, in your country.
2. Use the Internet Support Request form at http://support.digitallogic.ch/ → embedded products → New Support Request

Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!

1.7. Limited Two Year Warranty

DIGITAL-LOGIC AG guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, direct customers of DIGITAL-LOGIC AG, Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at http://support.digitallogic.ch/

All other customers must contact their local distributors for returning defective materials.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

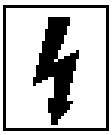
Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

1.8. Explanation of Symbols

CE Conformity
This symbol indicates that the product described in this manual is in compliance with all applied CE standards.

Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.



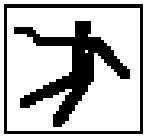
Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment

Warning, ESD Sensitive Device!
This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.

Attention!
This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.

Note...
This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.

Warning, Heat Sensitive Device!
This symbol indicates a heat sensitive component.



Safety Instructions
This symbol shows safety instructions for the operator to follow.

This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.

1.9. Applicable Documents and Standards

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems–Local and metropolitan area networks–Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. http://www.pc104.org
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

1.10. For Your Safety

Your new DIGITAL-LOGIC product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new DIGITAL-LOGIC product, please comply with the following guidelines.

Attention!
All work on this device must only be carried out by sufficiently skilled personnel.

Caution, Electric Shock!
Before installing your new DIGITAL-LOGIC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.

Warning, ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

1.11. RoHS Commitment

DIGITAL-LOGIC AG is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

1.11.1. RoHS Compatible Product Design

All DIGITAL-LOGIC standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all DIGITAL-LOGIC standard products.

1.11.2. RoHS Compliant Production Process

DIGITAL-LOGIC selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

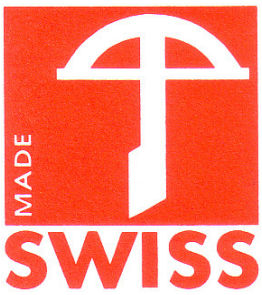
1.11.3. WEEE Application

The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since DIGITAL-LOGIC does not deliver ready-made products to end users the WEEE directive is not applicable for DIGITAL-LOGIC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

1.12. Swiss Quality



- 100% Made in Switzerland
- DIGITAL-LOGIC is a member of "Swiss-Label"
- This product was ***not*** manufactured by employees earning piecework wages
- This product was manufactured in humane work conditions
- All employees who worked on this product are paid customary Swiss market wages and are insured
- ISO 9000:2001 (quality management system)

1.13. The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

www.sqs.ch

The SQS Certificate ISO 9001:2000 has been issued to DIGITAL-LOGIC AG, the entire company, in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years at which time an audit is performed for recertification.

2. OVERVIEW

2.1. Standard Features

The smartCoreExpress is an electrical and mechanical definition for a COM or Computer on Module (miniaturized PC system), based on Intel's ATOM chip unit incorporating the major elements of a PC compatible computer.

- Powerful though low consumption ATOM CPU
- Soldered DDR2 RAM 512k up to 2GByte
- Single 220pin connectors (Tyco) for the smartCoreExpress BUS
- 5x x1 PCI-Express lanes
- 8x USB V2.0
- 1x PATA or (4x SATA plus 1x GE-LAN)
- 1x SDVO interface
- 1x LVDS 24bit interface
- 1x AC97 HAD interface
- 1x LPC BUS
- 1x SPI BUS
- 1x SM BUS
- 1x Generic Serial BUS (ex. CAN)
- 4x GPIO (programmable global in/out)
- Maximum Thermal Design Power up to 40W
- Reserved pins for: 1x Ethernet interface 1GE
- Single 5Volt supply
- Legacy signals for SuperIO

2.2. Technical Specifications

CPU	Specification
CoreDuo / Celeron M	Intel Atom 510 1.10GHz with 0.5MB L2-cache Intel Atom 530 1.60GHz with 0.5MB L2-cache
Clock	1.1 or 1.6GHz
1st Level Cache	2x 32kByte
2nd Level Cache	0.54 MByte (on die)
Technology	40nm
VCCCore @ 1.6GHz	1.050V
VCCCore @ 1.1GHz	0.844V
VCCCore @ deep sleep	0.748V
CPU BUS	CMOS
AGTL+ Termination	Not needed
FSB	533MHz quad-pumped synchronous BUS

Mathematics Coprocessor	
	Available on the Atom CPU

Intel US15W Graphics Memory Controller Hub	
Memory Controller	**Specification**
Supports	
Socket	DDR2 soldered memory
Technologies	DDR2-667
Capacity	512MByte up to 2GByte
Voltage	1.8V
Termination	0.9V
Width	64bit
ECC-Support	No

Intel US15W Graphics Memory Controller Hub	
Graphic Controller	**Specification**
Max. Video Memory	128MByte with Intel GMA
Graphic Core Frequency	250MHz
SDVO Port	2 channels (multiplexed with the PEG signals) 1x 200 Mpixel/sec Support for up to 1x DVI, 1x VGA and 1x LVDS Dotclock = 165MHz Compliant with DVI Spec.1.5
Flat Panel Interface	2 channel LVDS interface 1x 18, 2x 18, 1x 24, 2x 24bpp TFT Dotclock = up to 2x 112 MHz Resolutions 640 x 480 up to 1600 x 1200 (UXGA) Automatic panel detection via VESA EDID 1.3
LVDS 24bit	200Mpixel/sec

Intel US15W	Specification
PCIe BUS	2x x1 Lane
EIDE BUS	1x Ultra P-ATA 100
SATA BUS	-
USB V2.0	8 channel USB
APIC	INTEL I/O APIC
SMB	V2.0 SMBus controller
FWH	FirmWare Hub for BIOS devices
LPC	Serialized BUS (no ISA) used for external SuperI/O
Sound	AC97 2.3 HDA Interface with 192kHz sampling rate and 8 channels
IRQ Controller	8259 compatible
Timers	8254 compatible
Power Management	Integrated

Reset & Power Management	Specification
Controller	Atmel
Power Modes	S5, S3
ACPI	V3.0

BUS	Specification
LPC	8bit 33MHz
PCIexpress	2x x1 lane

Power Supply	Specification
DC Input	5.0V, max. 200mV ripple
Inrush Current	5.0V up to 2Amp for 100µs *
Standby Power	0.1W
Onboard Voltages	VCC Core, 1.05V, 1.8V, 0.9V, CoreVCC, 1.5V
Power Consumption	4W

* Use inductors in series to reduce the maximum inrush current!

Physical Characteristics	Specification
Dimensions	Length: 65 mm +/- 0.1mm Depth: 58 mm +/- 0.1mm Height: 11 mm +/- 0.2mm (with 5mm bus connectors) 14 mm +/- 0.2mm (with 8mm bus connectors) The connector height is selected by the connector on the carrier board.
Weight	70 gr / 8 ounces
PCB Thickness	1.6 mm / 0.0625 inches nominal
PCB Layer	Multilayer

Operating Environment	Specification
Relative Humidity	5-90% non-condensing
Vibration	5 to 2000 Hz
Shock	10 G
Operating Temperature	Standard: t.b.d. (depends on the CPU and the cooling concept) Extended Range: t.b.d.
Maximum Copper Temperature	90°C
Storage Temperature	-55°C to +85°C

EMI / EMC (IEC1131-2 refer MIL 461/462)	Specification
ESD Electro Static Discharge	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 Metallic protection needed Separate Ground Layer included 15 kV single peak
REF Radiated Electromagnetic Field	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. Not tested
EFT Electric Fast Transient (Burst)	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 Ohm, Ts = 5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2kV, 6 pulse/minute I/O: 500V, 2 pulse/minute FD, CRT: None
High-Frequency Radiation	EN55022

All information is subject to change without notice.

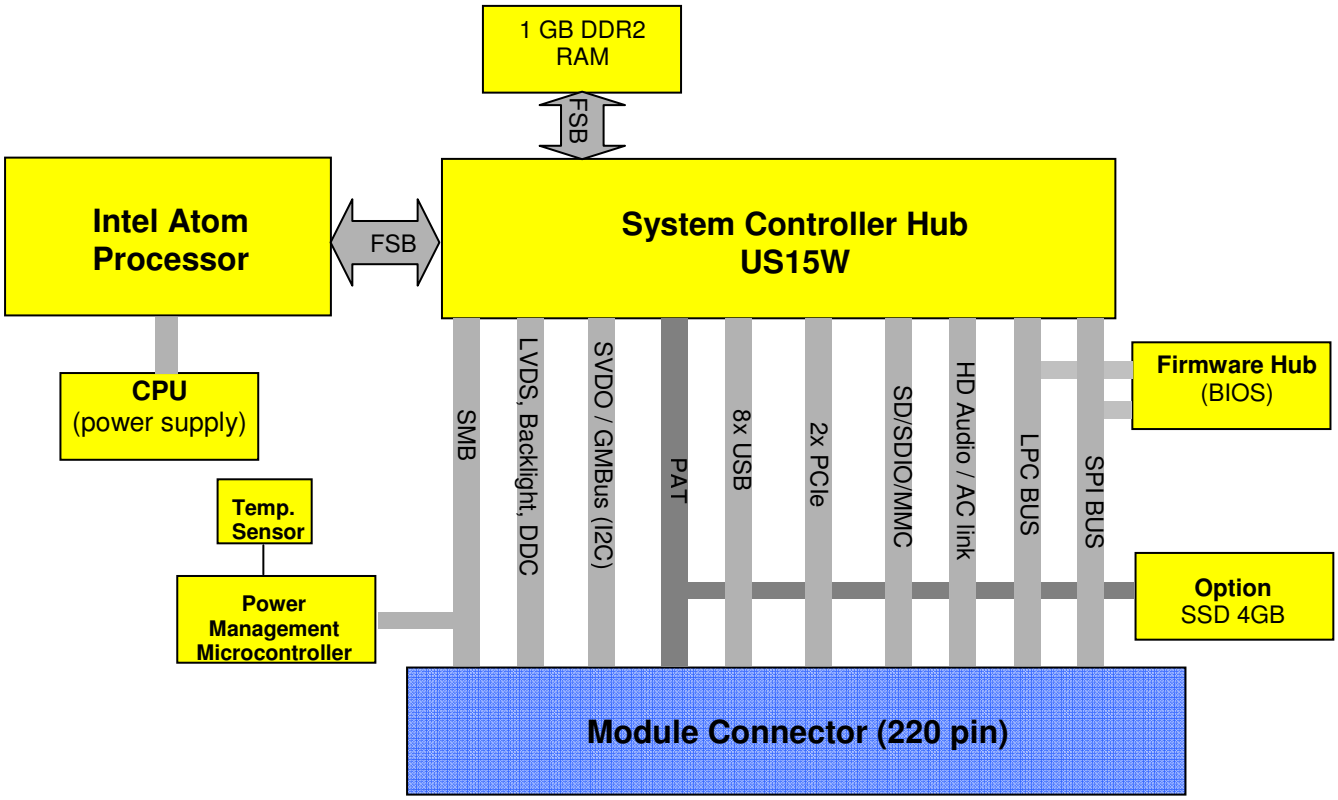
2.3. Examples of Ordering Codes

Product Name	Part Number	Description
SMA200-11G-xxGB		ATOM Z510, 1.1GHz
incl. 0.5GB RAM	805800	
incl. 1.0GB RAM	805801	
incl. 2.0GB RAM	805802	
SMA200-16G-xxGB		ATOM Z530, 1.6GHz
incl. 0.5GB RAM	805810	
incl. 1.0GB RAM	805811	
incl. 2.0GB RAM	805812	
SMA204-16G-xxGB		ATOM Z530, 1.6GHz, 4GB PATA SSD
incl. 0.5GB RAM	805820	
incl. 1.0GB RAM	805821	
incl. 2.0GB RAM	805822	
Options/Accessories		
SMX-CON5	807139	5mm COM Express connector
SMX-CON8	807138	8mm COM Express connector
SMA200DK	805850	SMA200 Development Kit

These are only examples; for current ordering codes, please see the current price list.

3. DIMENSIONS & DIAGRAMS

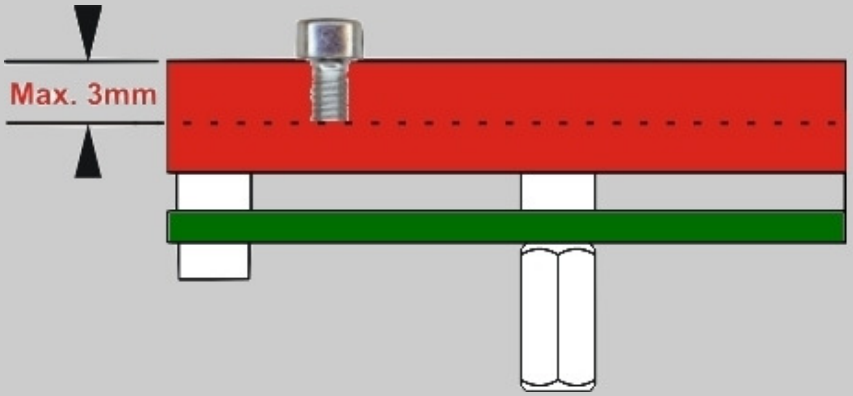
3.1. Block Diagram



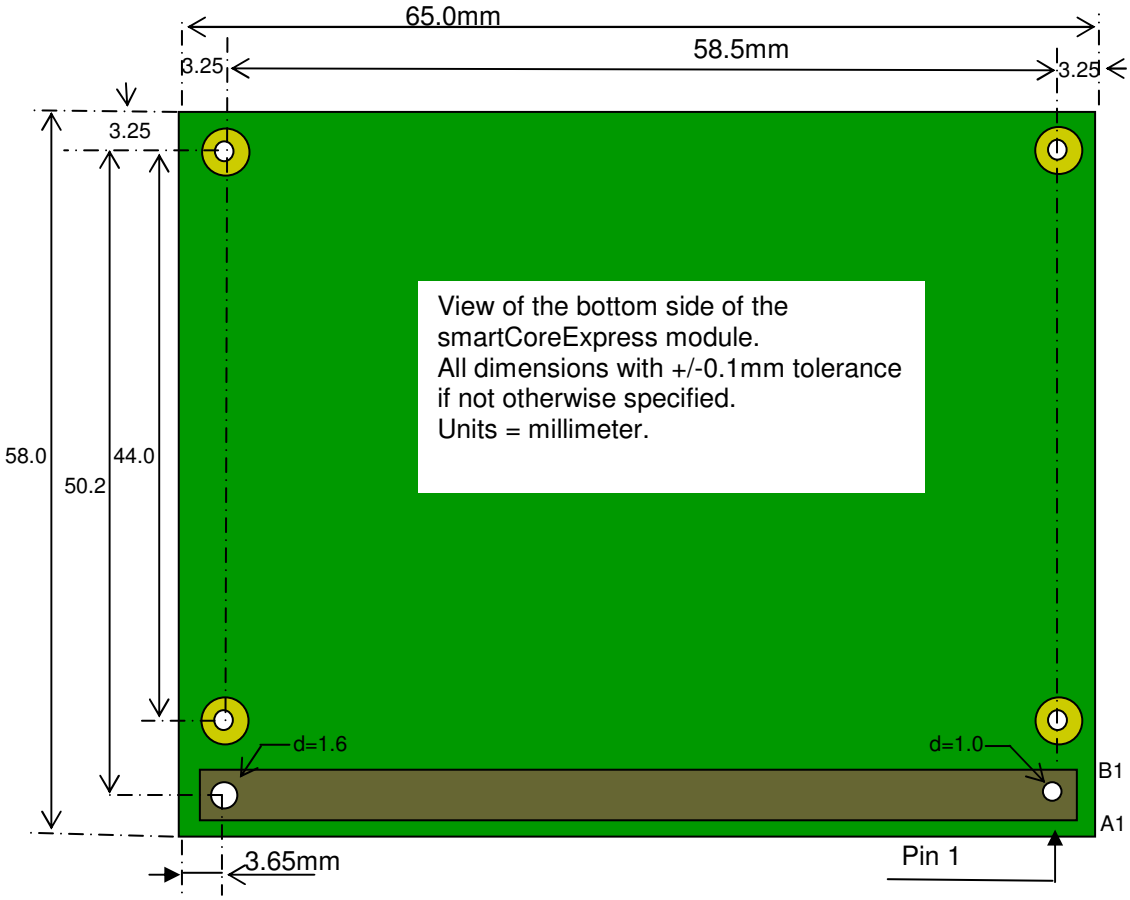
Design IN with the smartModule

Attention!
When using an active/passive heatsink that is **not** from DLAG, be very careful!

The maximum depth the screws can go into the product is 3mm or the module will be destroyed!

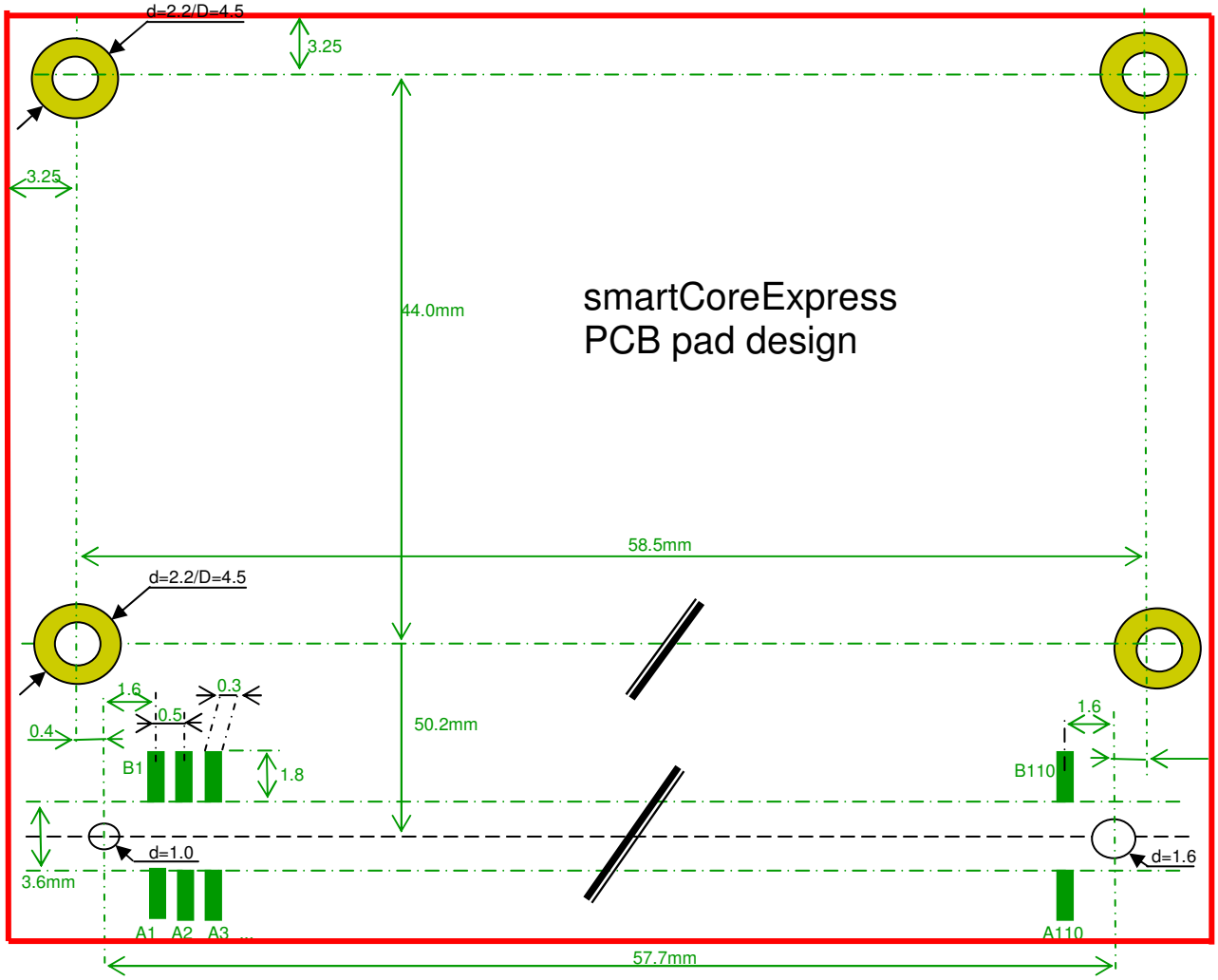


3.2. Dimensions of the smartCoreExpress Module

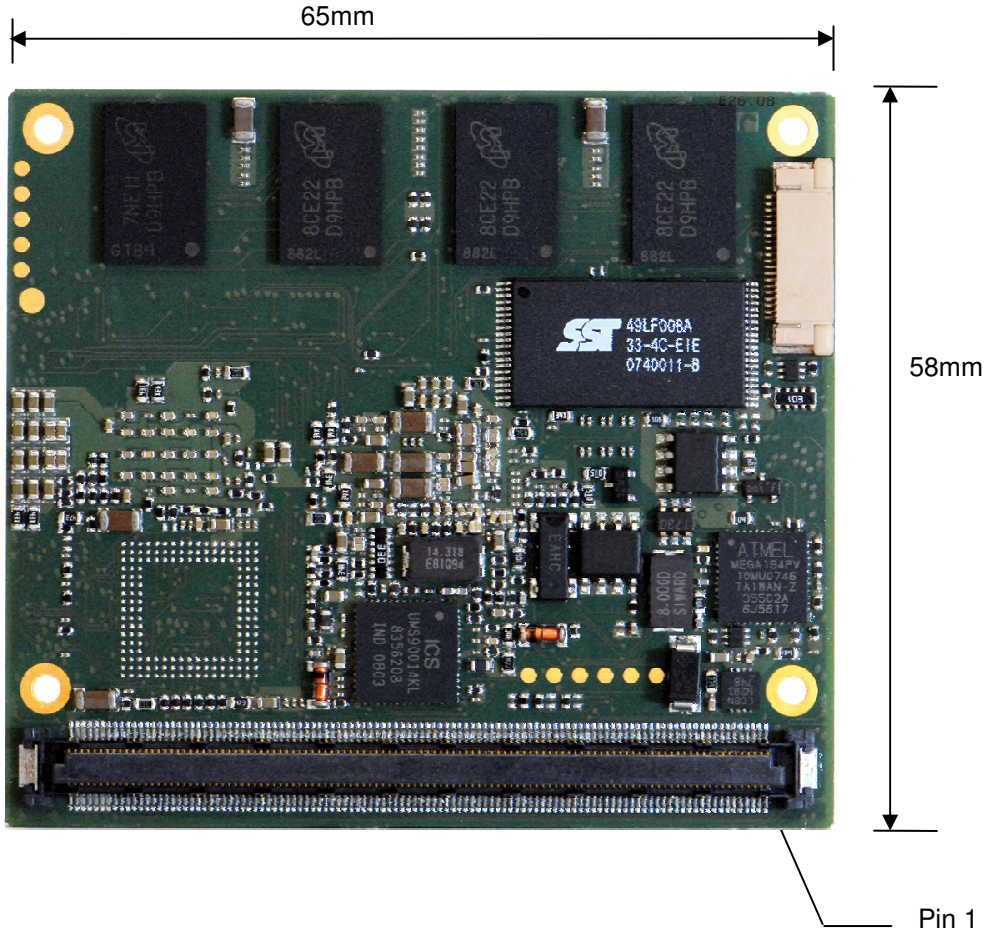


3.3. Connector Placement & Pin Definition on the Carrier Board

View of the Top Side (mounting side) of the smartCoreExpress PCB:



3.4. Photo of the Top Side of the PCB

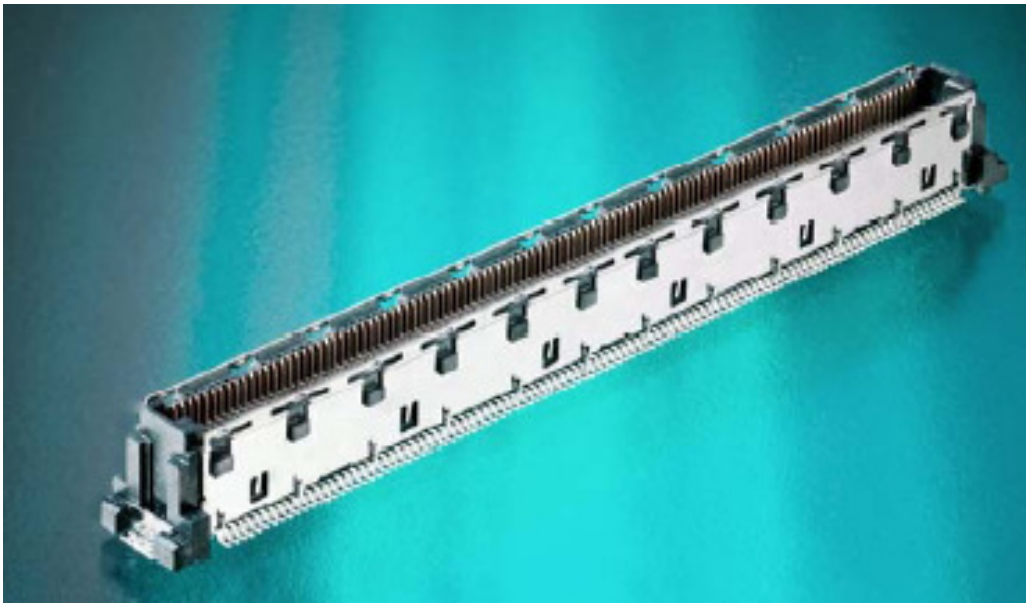


3.5. Dimensions of the Carrier Board Connector

SMX-CON8:

Standard Height: 5.0mm (Available alternative: 8.0mm)
DLAG Part Nr: 807138
AMP/Tyco: 8-6318491-6

(Components placed below the smartModule should total a maximum of 2.0mm.)



3.6. Component Heights between Module and Carrier Board

Parts mounted on the back side of the module (in the space between the bottom surface of the module PCB and the carrier board) should have a maximum height of 8.0mm.

4. COM-EXPRESS CONNECTOR DESCRIPTION

4.1. Signal Terminology Descriptions

Signal	Description
PU	Internally implemented pull up resistor
PD	Internally implemented pull down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant, active in standby state
O 3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power input/output
D	Differential signal pair
DDC	Display data channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA Specification, Revision 1.0a
LVDS	Low voltage differential signal: 350mV nominal; 450mV maximum differential signal
LAN	100/10Mbit/s LAN signals coming from the PHY
TPM	Trusted platform module
GE-LAN	1GB LAN signals

4.2. smartCoreExpress Connector Pinout

BUS on the smartCoreExpress – Connectors A / B: Pins 1-55

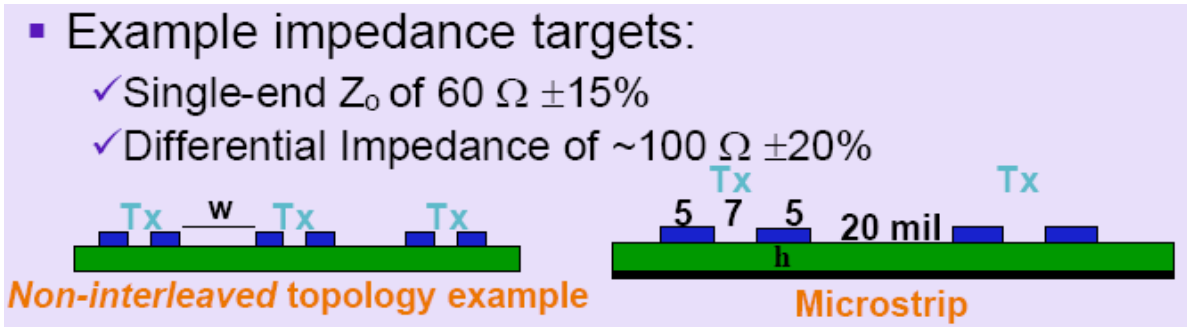
Pin	Signal	BUS	Type	Remarks	Pin	Signal	BUS	Type	Remarks
A1	GND				B1	GND			
A2	PCIe_TX0_N	PCIe	Dif	AC	B2	PCIe_RX0_N	PCIe	Dif	AC
A3	PCIe_TX0_P	PCIe	Dif	AC	B3	PCIe_RX0_P	PCIe	Dif	AC
A4	PCIe_CLK0_N	PCIe	Dif	AC	B4	PCIe_CLK1_N	PCIe	Dif	AC
A5	PCIe_CLK0_P	PCIe	Dif	AC	B5	PCIe_CLK1_P	PCIe	Dif	AC
A6	GND				B6	GND			
A7	PCIe_TX1_N	PCIe	Dif	AC	B7	PCIe_RX1_N	PCIe	Dif	AC
A8	PCIe_TX1_P	PCIe	Dif	AC	B8	PCIe_RX1_P	PCIe	Dif	AC
A9	PCIe_TX2_N	PCIe	Dif	AC	B9	PCIe_RX2_N	PCIe	Dif	AC
A10	PCIe_TX2_P	PCIe	Dif	AC	B10	PCIe_RX2_P	PCIe	Dif	AC
A11	GND				B11	GND			
A12	PCIe_CLK2_N	PCIe	Dif	AC	B12	PCIe_CLK3_N	PCIe	Dif	AC
A13	PCIe_CLK2_P	PCIe	Dif	AC	B13	PCIe_CLK3_P	PCIe	Dif	AC
A14	PCIe_TX3_N	PCIe	Dif	AC	B14	PCIe_RX3_N	PCIe	Dif	AC
A15	PCIe_TX3_P	PCIe	Dif	AC	B15	PCIe_RX3_P	PCIe	Dif	AC
A16	GND				B16	GND			
A17	PCIe_REQ0#	PCIe	3.3v-O	Clk request	B17	PCIe_REQ1#	PCIe	3.3v-O	Clock request
A18	PCIe_REQ2#	PCIe	3.3v-O	Clk request	B18	PCIe_REQ3#	PCIe	3.3v-O	Clock request
A19	SDVO_CLK_N	SDVO	Dif	AC	B19	SDVO_INT_N	SDVO	Dif	AC
A20	SDVO_CLK_P	SDVO	Dif	AC	B20	SDVO_INT_P	SDVO	Dif	AC
A21	GND				B21	GND			
A22	SDVO_GREEN_N	SDVO	Dif	AC	B22	SDVO_BLUE_N	SDVO	Dif	AC
A23	SDVO_GREEN_P	SDVO	Dif	AC	B23	SDVO_BLUE_P	SDVO	Dif	AC
A24	SDVO_TVCLK_N	SDVO	Dif	AC	B24	SDVO_STALL_N	SDVO	Dif	AC
A25	SDVO_TVCLK_P	SDVO	Dif	AC	B25	SDVO_STALL_P	SDVO	Dif	AC
A26	GND				B26	GND			
A27	SDVO_RED_N	SDVO	Dif	AC	B27	SDVO_DDC_CLK	SDVO	3.3V	Bidir.
A28	SDVO_RED_P	SDVO	Dif	AC	B28	SDVO_DDC_DAT	SDVO	3.3V	Bidir.
A29	LVDS_D0_P	LVDS	Dif	LV	B29	LVDS_D1_P	LVDS	Dif	LV
A30	LVDS_D0_N	LVDS	Dif	LV	B30	LVDS_D1_N	LVDS	Dif	LV
A31	GND				B31	GND			
A32	LVDS_D2_P	LVDS	Dif	LV	B32	LVDS_CLK_P	LVDS	Dif	LV
A33	LVDS_D2_N	LVDS	Dif	LV	B33	LVDS_CLK_N	LVDS	Dif	LV
A34	LVDS_D3_P	LVDS	Dif	LV	B34	LVDS_BKL_CTR	LVDS	3.3v	
A35	LVDS_D3_N	LVDS	Dif	LV	B35	LVDS_BKL_EN	LVDS	3.3v	
A36	GND				B36	LVDS_DETECT#	LVDS	3.3V	
A37	LVDS_DDC_DAT	LVDS	3.3v		B37	LVDS_VDD_EN	LVDS	3.3V	
A38	LVDS_DDC_CLK	LVDS	3.3v		B38	USB_C_DEV	USB	3.3V	
A39	USB_0_P	USB	Dif	LV	B39	USB_1_P	USB	Dif	LV
A40	USB_0_N	USB	Dif	LV	B40	USB_1_N	USB	Dif	LV
A41	GND				B41	GND			
A42	USB_2_P	USB	Dif	LV	B42	USB_3_P	USB	Dif	LV
A43	USB_2_N	USB	Dif	LV	B43	USB_3_N	USB	Dif	LV
A44	USB_4_P	USB	Dif	LV	B44	USB_5_P	USB	Dif	LV
A45	USB_4_N	USB	Dif	LV	B45	USB_5_N	USB	Dif	LV
A46	GND				B46	GND			
A47	USB_6_P	USB	Dif	LV	B47	USB_7_P	USB	Dif	LV
A48	USB_6_N	USB	Dif	LV	B48	USB_7_N	USB	Dif	LV
A49	USB_OC01#	USB	3.3v		B49	USB_OC23#	USB	3.3v	
A50	USB_OC45#	USB	3.3v		B50	USB_OC67#	USB	3.3v	
A51	GND				B51	GND			
A52	GE_CLK	GE-LAN			B52	GE_RTS	GE-LAN		
A53	GE_TX0	GE-LAN			B53	GE_RX0	GE-LAN		
A54	GE_TX1	GE-LAN			B54	GE_RX1	GE-LAN		
A55	GE_TX2	GE-LAN			B55	GE_RX2	GE-LAN		

BUS on the smartCoreExpress – Connectors A / B: Pins 56-110

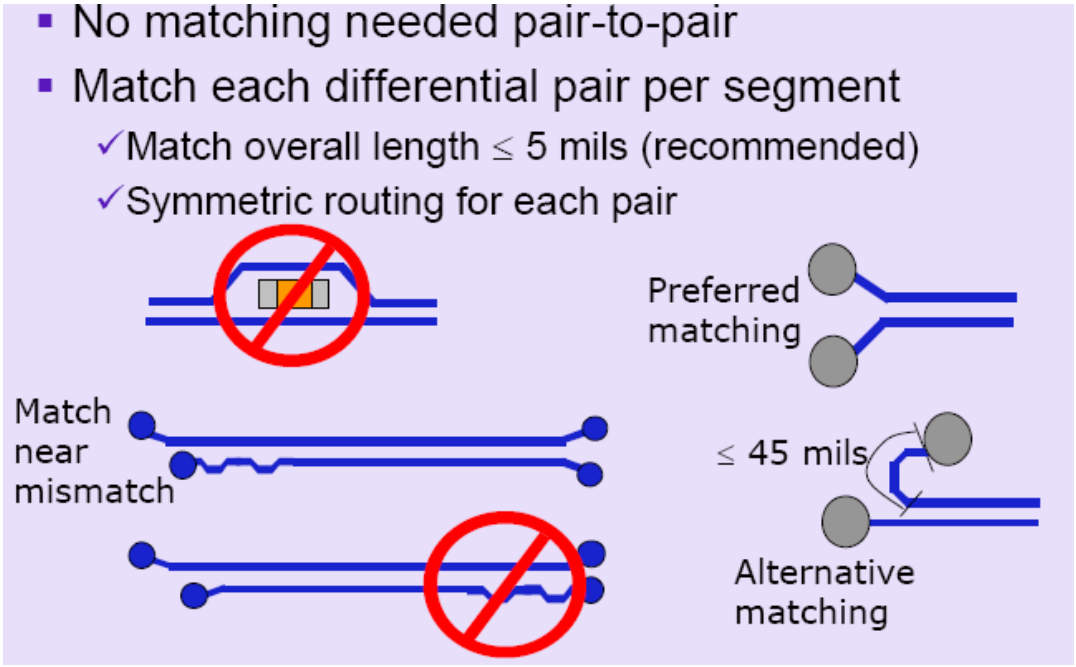
Pin	Signal	BUS	Type	Remarks	Pin	Signal	BUS	Type	Remarks
A56	SMB_CLK	SMB	3.3V	bidir	B56	SPI_MISO	SPI	3.3V	Bidir.
A57	SMB_DAT	SMB	3.3V	bidir	B57	SPI_MOSI	SPI	3.3V	Bidir
A58	SMB_ALERT#	SMB	3.3V	bidir	B58	SPI-CS#	SPI	3.3Vo	
A59	SATA_LED#	SAT	3.3Vo		B59	SPI_CLK	SPI	3.3Vo	
A60	GND				B60	GND			
A61	IDE_D3 / SATA_Tx0P	HD	5 /DI		B61	IDE_CS3 / SATA_Tx0P	HD	5 /DI	
A62	IDE_A0 / SATA_Tx0N	HD	5 /Di		B62	IDE_DAK / SATA_Tx0N	HD	5 /Di	
A63	IDE_A2 / SATA_Rx0P	HD	5 /Di		B63	IDE_D4 / SATA_Rx0P	HD	5 /Di	
A64	IDE_D8 / SATA_Rx0N	HD	5 /Di		B64	IDE_D2 / SATA_Rx0N	HD	5 /Di	
A65	IDERQ / GND	HD	5 /		B65	IDEIORDY / GND	HD	5 /	
A66	IDE_A1 / SATA_Tx2P	HD	5 /Di		B66	IDE_D10 / SATA_Tx2P	HD	5 /Di	
A67	IDE_D13 / SATA_Tx2N	HD	5 /Di		B67	IDE_D6 / SATA_Tx2N	HD	5 /Di	
A68	IDE_D1 / SATA_Rx2P	HD	5 /Di		B68	IDE_D12 / SATA_Rx2P	HD	5 /Di	
A69	IDE_IRQ / SATA_Rx2N	HD	5 /Di		B69	IDE_D9 / SATA_Rx2N	HD	5 /Di	
A70	GND				B70	GND			
A71	IDE_D11 / PCIE_TX4_N	HD	5 /Di		B71	IDE_D15 / PCIE_RX4_N	HD	5 /Di	
A72	IDE_D5 / PCIE_TX4_N	HD	5 /Di		B72	IDE_D0 / PCIE_RX4_N	HD	5 /Di	
A73	IDE_RD# / PCIE_REQ4	HD	5 / 3		B73	IDE_D7	HD	5	
A74	IDE_D14/ PCIE_CK4_N	HD	5 /Di		B74	IDE_WR#/ CAN_TX	HD	5 /Di	
A75	IDE_CS1/ PCIE_CK4_N	HD	5 /Di		B75	IDE_DET / CAN_RX	HD	5 /Di	
A76	LPC_AD3	LPC	3.3V		B76	LPC_CLK0	LPC	3.3Vo	33MHz
A77	LPC_AD1	LPC	3.3V		B77	LPC_CLK1	LPC	3.3Vo	33MHz
A78	LPC_AD0	LPC	3.3V		B78	LPC_SERIRQ	LPC	3.3V	
A79	LPC_FRAME#	LPC	3.3V		B79	LPC_AD2	LPC	3.3V	
A80	GND				B80	GND			
A81	SD_WP	SDIO	3.3V		B81	SD_DATA7	SDIO	3.3V	
A82	SD_CD#	SDIO	3.3V		B82	SD_PWR*	SDIO	3.3V	
A83	SD_CLK	SDIO	3.3V		B83	SD_DATA2	SDIO	3.3V	
A84	SD_DATA1	SDIO	3.3V		B84	SD_LED	SDIO	3.3V	
A85	SD_DATA3	SDIO	3.3V		B85	SD_DATA4	SDIO	3.3V	
A86	SD_DATA5	SDIO	3.3V		B86	SD_DATA0	SDIO	3.3V	
A87	SD_DATA6	SDIO	3.3V		B87	SD_CMD	SDIO	3.3V	
A88	LVDS_CTLB_DAT	LVDS	3.3Vo		B88	BIOS_Recovery / WDO	SYS	3.3Vo	
A89	LVDS_CTLB_CLK	LVDS	3.3Vo		B89	Speaker Output	SYS	3.3Vo	
A90	GND				B90	GND			
A91	AC97_DOCK_EN#	HDA	3.3Vi		B91	AC97_BITCLK	HDA	3.3Vo	
A92	AC97_SDATAIN1	HDA	3.3V		B92	AC97_DOCK_RST#	HDA	3.3Vo	
A93	AC97_SDATAOUT	HDA	3.3V		B93	AC97_SDATAIN0	HDA	3.3V	
A94	AC97_RST#	HDA	3.3Vo		B94	AC97_SYNC	HDA	3.3V	
A95	IDE_PCSEL	HD	5V		B95	A20M#	SYS	5V	
A96	GPIO0	SYS	3.3V		B96	Powergood	SYS	5Vi	
A97	GPIO1	SYS	3.3V		B97	PSON#	SYS	3.3Vi	
A98	GPIO2	SYS	3.3V		B98	PWRBTN#	SYS	3.3Vi	
A99	GPIO3	SYS	3.3V		B99	SUS_S3#_Output	SYS	3.3Vo	
A100	GND				B100	GND			
A101	Reset_Output#	SYS	3.3Vo		B101	SUS_S4&5#_Output	SYS	3.3Vo	
A102	Reset_Input#	SYS	3.3Vi		B102	BIOS_Disable#	SYS	3.3Vi	
A103	WAKE_Input#	SYS	3.3Vi		B103	Battery Supply 3.0-3.6V	SYS	3Vin	
A104	+5Volt Supply Input	PWR	5Vi		B104	+5Volt_Always Input	PWR	5Vi	
A105	+5Volt Supply Input	PWR	5Vi		B105	+5Volt Supply Input	PWR	5Vi	
A106	+5Volt Supply Input	PWR	5Vi		B106	+5Volt Supply Input	PWR	5Vi	
A107	+5Volt Supply Input	PWR	5Vi		B107	+5Volt Supply Input	PWR	5Vi	
A108	+5Volt Supply Input	PWR	5Vi		B108	+5Volt Supply Input	PWR	5Vi	
A109	+5Volt Supply Input	PWR	5Vi		B109	+5Volt Supply Input	PWR	5Vi	
A110	GND				B110	GND			

5. SIGNAL DESCRIPTIONS OF THE SMARTCOREEXPRESS

5.1. Wire Design for Typical Impedances

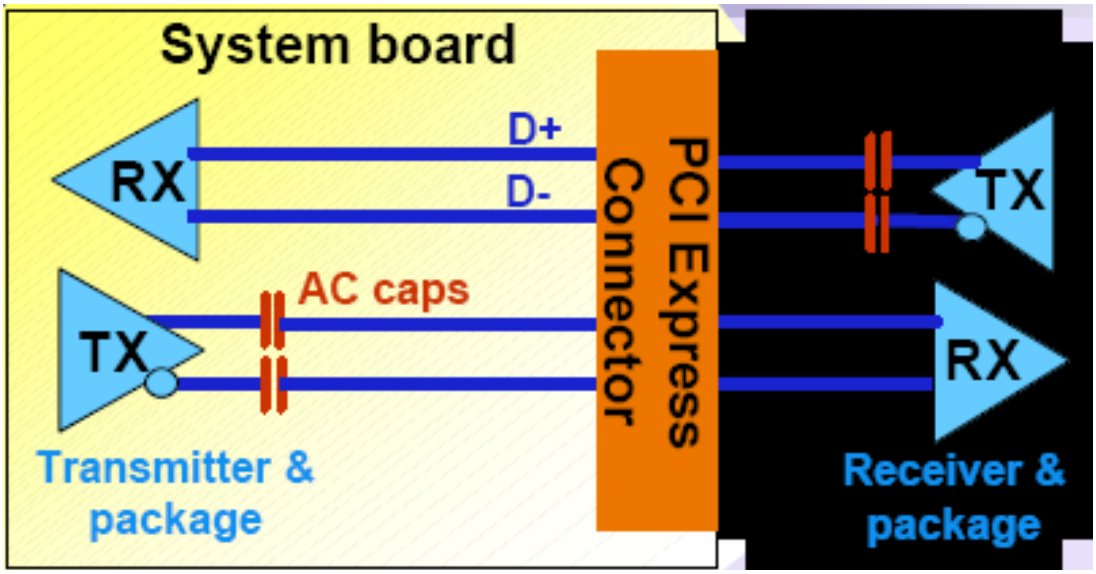


5.2. Matching of the Differential Pairs

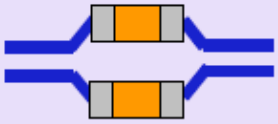


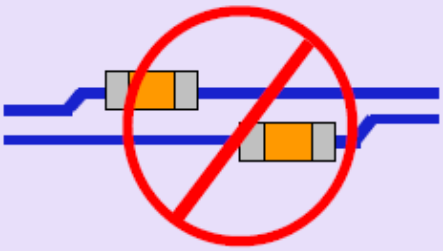
5.3. Placing an AC Coupling Capacitor on each PCIe-TX

In the smartCoreExpress module, all PCI-TX pairs already include the series AC capacitors.



- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement best





- Cap size: 0.1uF best
- Same sizes for both D+/D-
- Cap location:
  - ✓Along Tx pairs on system board
  - ✓Along Tx pairs on add-in card

5.4. smartCoreExpress Signal Groups

5.4.1. PCI-Express

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
PCIe_Tx [0-4] +/-	PCIe	Dif Out	Transmitter 2.5Gbit Connected to an Rx pin pair of the device.	100nF Series Cap.	-	200	100	0.2
PCIe_Rx [0..4] +/-	PCIe	Dif In	Receiver 2.5Gbit Connected to a Tx pin pair of the device. The Tx output of the device needs an AC coupling capacitor.	-	Series Cap. 100nF As 0402	200	100	0.2
PCIe_CLK[0..4] +/-	PCIe	Dif Out	Reference clock (100MHz) Connected to a Refclock pin pair of the device.	-	-	200	100	0.2
PCIe_REQ#[0..4]	PCIe	3.3V In	A low signal at this input will enable the PCI-Clk-Output of the corresponding PCI-Express lane.	PU integrated in the CK540	-	200	Static	-

If the signals are not used:

All these PCI-Express signals may be left open.

Remarks:

Pair to Pair spacing: 35mil = 0.9mm
BUS to BUS spacing: 20mil = 0.5mm

The AC coupling capacitors must be placed near the device for the Tx signals only. The maximum number of vias per signal is less than 4.

EMV/EMI filters:

Are not needed.

5.4.2. SDVO

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
SDVO_CTRLCLK	SDVO	*	DDC signal	PU 4.7k to 3.3V			55	
SDVO_CTRLDAT	SDVO	*	DDC signal	PU 4.7K to 3.3V			55	
SDVO_CLK +/-	SDVO	Dif Out	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_INIT +/-	SDVO	Dif In	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_STALL +/-	SDVO	Dif In	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_TVCLKIN +/-	SDVO	Dif In	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_Red +/-	SDVO	Dif Out	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_Green +/-	SDVO	Dif Out	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5
SDVO_Blue +/-	SDVO	Dif Out	Needs a series 100nF capacitor to connect to an SDVO converter chip	-	-	100	100	0.5

If the signals are not used:

All these SDVO signals may be left open.

Remarks:

For the DDC signals, a voltage translator to 3.3V or 5V is needed.

Pair to Pair spacing: 35mil = 0.9mm
Pair to Pair matching: better than 25mm
BUS to BUS spacing: 20mil = 0.5mm

The AC coupling capacitors (100nF / 0402) must be placed near the device for the Tx signals only.
The maximum number of vias per signal is less than 4.

Supported devices:

SiliConImage SIL1362 / SIL1364 (DVI)
Chrontel CH7021 (SDTV / HDTV / CRT)

EMV/EMI filters:

Chokes are needed.

5.4.3. LVDS

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
LVDS_DDCCLK	LVDS	3.3V	DDC signal	PU 10k to 3.3V	-	150	55	
LVDS_DDCDAT	LVDS	3.3V	DDC signal	PU 10k to 3.3V	-	150	55	
LVDS_DATA[0..3] +/-	LVDS	Dif Out	LVDS data signal Connected directly to the display.	-	-	150	100	0.5
LVDS_CLK +/-	LVDS	Dif Out	LVDS clock signal Connected directly to the display.	-	-	150	100	0.5
LVDS_VDDEN	LVDS	3.3V Out	LVDS control signal To switch on/off the VDD of the LVDS display.	100k pull down	-	150	55	
LVDS_BKLCTL	LVDS	3.3V Out	Connected to the LVDS display's PWM-based backlight inverter module. No multi-bus master mode is supported.		-	150	55	
LVDS_BKLEN	LVDS	3.3V Out	Connected to the LVDS display's backlight inverter module switch.	100k pull down	-	150	55	
LVDS_CTLA_CLK	LVDS	3.3V I/O	Connected to the LVDS display's PWM-based backlight inverter module. No multi bus master mode supported.	PU 4.7k to 3.3V	-	150	55	
LVDS_CTLB_DATA	LVDS	3.3V I/O	Connected to the LVDS display's PWM-based backlight inverter module.	PU 4.7k to 3.3V	-	150	55	

If the signals are not used:

All these LVDS signals may be left open.

Remarks:

For the DDC signals, a voltage translator to 3.3V or 5V is needed.

Pair to Pair spacing: 35mil = 0.9mm
Pair to Pair matching: better than 25mm
Bus to Bus spacing: 20mil = 0.5mm

Maximum via count: 0 2.

EMV/EMI filters:

5.4.4. USB

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
USB_[0..7] +/-	USB	Dif	Differential USB data signal pair	-	-	300	100	0.2
USB_OC[0..7]#	USB	3.3V In	USB overcurrent signal	PU 10k to 3.3V	-	300	55	

If the signals are not used:

All these USB signals may be left open.

Remarks:

EMV/EMI-filters:

Use a choke and clamping diode on each signal pair.

5.4.5. Parallel ATA

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
PATA_D[15..0]	CMOS	5V I/O	IDE data signals	Series 33	-	100	55	-
PATA_A[0..2]	CMOS	5V Out	IDE address signal. Connect directly to the PATA device.	-	-	100	55	
PATA_IOR#]	CMOS	5V Out	IDE control signal. Connect directly to the PATA-device.	-	-	100	55	
PATA_IOW#]	CMOS	5V Out	IDE control signal. Connect directly to the PATA-device.	-	-	100	55	
PATA_DACK#]	CMOS	5V Out	IDE control signal. Connect directly to the PATA-device.	-	-	100	55	
PATA_CS[3,1]	CMOS	5V Out	IDE control signal. Connect directly to the PATA-device.	-	-	100	55	
PATA_REQ	CMOS	3/5V In	IDE control signal. Connect directly to the PATA-device.	-	-	100	55	
PATA_IORDY	CMOS	3V In	IDE control signal. Connect directly to the PATA-device.	PU 4.7k to 3.3V	-	100	55	
PATA_IRQ	CMOS	3V In	IDE control signal. Connect directly to the PATA-device.	PU 10k to 3.3V	-	100	55	
PATA_PCSEL	CMOS	3V In	GND = SSD works as master HIGH = SSD works as slave	PD 4.7k to GND		100	55	

If the signals are not used:

All this PATA signals may be left open.

Remarks:

EMV/EMI filters:

Are not needed.

5.4.6. LPC BUS

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
LPC_FRAME#	CMOS	3.3V Out	Connect to the LPC device	-	-	100	55	-
LPC_AD[3..0]	CMOS	3.3V I/O	Connect to the LPC device	-	-	100	55	-
LPC_SERIRQ	CMOS	3.3V I/O	Connect to the LPC device	PU 10k to 3.3V	-	100	55	-
LPC_CLKOUT[0..1]	CMOS	3.3V Out	Connect to the Firmware hub or the SuperIO	Series 33 Ohm	-	100	55	-

If the signals are not used:

Leave the pins open.

Remarks:

Use 33 Ohm series termination in each LPC-CLKx-signal.

The LPC_CLKOUTx may drive only 2 loads.

EMV/EMI filters:

Are not needed.

5.4.7. SMBus

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
SMB_ALERT#	CMOS	3.3V In	Connect to the SMB device	PU 10k to 3.3V	-	200	55	-
SMB_DATA	CMOS	3.3V I/O	Connect to the SMB device open drain	PU 4.7k to 3.3V	-	200	55	-
SMB_CLOCK	CMOS	3.3V I/O	Connect to the SMB device open drain	PU 4.7k to 3.3V	-	200	55	-

If the signals are not used:

The pins can stay open.

Remarks:

The SMB_ALERT# may be used to initiate an SMB event over APIC or an SMI.

Maximum BUS capacitance is 200pF. For higher BUS loads, the SMB repeater PCA9515 from Philips is recommended. Each new SMB segment must be terminated with 2x 4.7k.

EMV/EMI filters:

Are not needed.

5.4.8. HDA Audio Interface

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
HDA_DOCKEN#	CMOS	3.3V Out	HAD dock enable. This signal controls the external HD audio docking isolation logic. When de-asserted, the switch is in isolate mode.	-	-	200	55	-
HAD_RST#	CMOS	3.3V Out	Reset signals for the external codecs.	Series 33	-	200	55	-
HAD_SYNC	CMOS	3.3V Out	Sample rate at 48kHz to the codecs.	Series 33		200	55	-
HAD_BITCLK	CMOS	3.3V Out	24MHz signal for the external codec.	Series 33		200	55	-
HAD_SDATAin [1..0]	CMOS	3.3V In	Data input from the external codecs.	-	Series 33 Ohm	200	55	-
HAD_SDATAout	CMOS	3.3V Out	Data output from the ext. PC.	Series 33				
HAD_DOCKRST#	CMOS	3.3V	Reset signal for the codecs.	-	-	200	55	-

If the signals are not used:

Remarks:

The 33 Ohm series termination should be placed directly next to the codecs.

Supported Codecs:

EMV/EMI filters:

Are not needed.

5.4.9. SD / SDIO Interface

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
SD0_CD#	CMOS	3.3V Out	Connect to an SDIO device or card.	PU 10k to 3.3V	-	100	55	-
SD0_CLK	CMOS	3.3V Out	Connects to the pin of the SD/SDIO device or card.	Series 47 Ohm	Series 49 Ohm	100	55	
SD0_CMD#	CMOS	3.3V I/O	Connects to the pin of the SD/SDIO device or card.	PU 10k to 3.3V Series 47		100	55	
SD_Data [3..0]	CMOS	3.3V	Connects to the pin of the SD/SDIO device or card.		Series 49 Ohm	100	55	
SD0_LED	CMOS	3.3V Out	Optional.					
SD0_PWR#	CMOS	Out	Connect to the power pin on the SD/SDIO device or card, voltage translation might be required.					
SD0_WP	CMOS	In	Connects to the pin of the SD/SDIO device or card.	PU 10k to 3.3V				

If the signals are not used:

Remarks:

EMV/EMI filters:

Are not needed.

5.4.10. SPI BUS

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
SPI_MISO	CMOS	3.3V In	Connect to the SPI device.		-	150	55	-
SPI_MOSI	CMOS	3.3V Out	Connect to the SPI device.			150	55	-
SPI_CLK	CMOS	3.3V Out	Connect to the SPI device. f = 17.86 and 31.25MHz	Series 33 Ohm		150	55	-
SPI_CS#	CMOS	3.3V Out	Connect to the SPI device.			150	55	-

If the signals are not used:

Remarks:

EMV/EMI filters:

Are not needed.

5.4.11. SATA Interface (Option)

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
SATA_Tx[0..3]	SATA	Dif	SATA transmitter pair		Series 10nF	100	100	-
SATA_Rx[0..3]	SATA	Dif	SATA receiver pair		Series 10nF	100	100	-

If the signals are not used:

Unused SATA interfaces may be open.

Remarks:

The 10nF capacitors 0402 need to be placed directly at the SATA connector.
Maximum via count is 2 per signal.
BUS to BUS spacing is min. 20mil = 0.5mm
Pair to Pair spacing is min. 35mil = 0.9mm

The SATA_LED# output show the SATA (all ports) activity. The LED must be connected to +3.3V with a series resistor of 330 Ohm to the “SATA_LED#” signal.

EMV/EMI filters:

Are not needed.

5.4.12. GLAN

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
GLAN_TX +/-	GLAN	Dif	GLAN TX pair for 1GE	-	100nF	250	95	0.5
GLAN_RX +/-	GLAN	Dif	GLAN RX pair for 1GE	-	100nF	250	95	0.5
GLAN-CLK +/-	GLAN	Dif	GLAN reference clock pair	-	33 Ohm	250	50	-
LCI_TXD[2..0]	LCI	3.3V Out	3x TX signal for 10/100MB	-	-	250	50	-
LCI_RXD[2..0]	LCI	3.3V In	3x RX signal for 10/100MB	-	-	250	50	-
LCI_RST	LCI	3.3V Out	LAN reset/synch	-	-	250	50	-

If the signals are not used:

Unused GLAN /LCI interfaces may be open.

Remarks:

The 10nF capacitors 0402 need to be placed directly at the SATA connector.
Maximum via count is 2 per signal.
BUS to BUS spacing is min. 20mil = 0.5mm
Pair to Pair spacing is min. 35mil = 0.9mm

EMV/EMI filters:

Are not needed.

5.4.13. CAN / Serial

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
CAN_TX	CMOS	3.3V Out	Serial output.	Res.	-	-	-	-
CAN_RX	CMOS	3.3V In	Serial input.	Res.	-	-	-	-

If the signals are not used:

Unused interfaces may be open.

Remarks:

EMV/EMI filters:

Are not needed.

5.4.14. PM

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
WAKE#	CMOS	3.3V In	To wakeup the system, this input must be pulled to GND.	PU 1k0k 3.3V	-	-	-	-
WD_OUT	CMOS	3.3V Out	Indicates a watchdog timeout event with a high level. Cleared with a reset and at power-on.	-	-	-	-	-
SUS_S3#	CMOS	3.3V Out	Low = system is in suspend state S3/S4/S5 (ACPI).	-	-	-	-	-
SUS_S4&5#	CMOS	3.3V Out	Low = system is in suspend state S4/S5 (ACPI).	-	-	-	-	-
GPIO[3..0]	CMOS	3.3V I/O	General purpose I/O pin.	-	-	-	-	-
RST_IN#	CMOS	3.3V In	To reset the system, this input must be pulled to GND.	PU 10k to 3.3V	-	-	-	-
RST_OUT#	CMOS	3.3V Out	Goes low during the reset phase and stays at high in the running phase.	-	-	-	-	-
Power-Good	CMOS	3.3V In	High = feedback from the external power supplies, that the voltages are in the valid ranges.	PU 10k to 3.3V	-	-	-	-
PS_ON	CMOS	3.3V Out	High = power supply on the baseboard is switched on.	-	-	-	-	-
PWRBTN#	CMOS	3.3V In	To activate this signal, the PWR_BTN# must be pulled to GND.	PU 1k to 3.3V				
BIOS_Disable#	CMOS	3.3V In	Low = onmodule BIOs is disabled, an external BIOS may be connected over LPC.	PU 1k to 3.3V	-	-	-	-
A20M#	CMOS	3.3V In	Connect to the SuperIO's KBC to switch between real and protected mode.	PU 100k to 5.0V	-	-	-	-
Speaker	CMOS	3.3V Out	Speaker					

If the signals are not used:

Leave the signal open.

Remarks:

EMV/EMI filters:

Are not needed.

5.4.15. Supply

Signal	BUS	Type	Description	On Module Termination	Ext. Termination Needed	Max. Length in mm	Ohm	Matched Length in mm
+5Volt	PWR	In	5V power supply input. Switched with the sus4signal	-	-	-	-	-
+5V Always	PWR	In	5V Always available.					
VCCRTC	PWR	In	RTC supply 3.0-3.6Volt. Connect to a lithium battery, using a 1k series resistor.					

6. SMARTCORE-EXPRESS CONNECTOR SPECIFICATIONS

The connector type is equal to the COMexpress connector. This is a 220pin, surface-mounted connector with 0.5mm pitch.

Parameter	Condition	Specification
Material	Contact	Copper alloy
	Housing	Thermoplast molded compound LCP
Electrical	Current	0.5 Amp
	Voltage	50 VAC
	Termination Resistance	55mΩ max. ΔR = 20mΩ max.
	Insulation Resistance	500MΩ
Mechanical	Mating Cycles	30
	Connector Mating Force	0.9N per contact
	Connector Un-mating Force	0.1N per contact
	Pitch	0.5mm
	Number of pins	220
	Temperature rating	-40°C to 85°C

The manufacturer of the connector is:

Source on smartCore *	Part Name	Part Number
Carrier Board Connector		
TYCO / AMP	H = 8mm Alternative H = 5mm Standard	8-6318491-6 3-1827253-6
smartCoreExpress Module Connector		
TYCO / AMP	Mating connector	8-1318490-6

The stack height may be defined on the carrier board as either 5 or 8mm using the two different connector types available.

7. SMARTCORE-EXPRESS VERSUS COMEXPRESS

The smartCoreExpress supports small footprints and especially mobile applications. It is powered by the modern Intel Atom CPU technology.

To select the correct module, this chapter compares the different PCIe-based module concepts. All concepts allow minimum (required) and maximum (optional) features.

The following table summarizes the features of all PCIe COMs.

Examples: 2 / 6 = 2 required, 6 optional from each module
1 / 1 (PCIe) = 1 required, no more optional, 1x PCI lane needed.
Depending on the concept, reduces the number of free PCIe lanes.

Features	SmartCore Express	ETXexpress COMexpress Type 2 Basic form factor	MicroETXexpress COMexpress Type 2 Small form factor	NanoETXexpress COMexpress Type 1	Q-Seven
Size [mm]	58 x 65 3770mm2 h = 5 + 6mm	95 x 125 11875mm2 h = 8 + 13mm	95 x 95 9025mm2 h = 5 + 13mm	51 x 80 4080mm2 h = 5 + 13mm	70 x 70 4900mm2 h = 12mm
Supply Input	5V typ. 5W	12V typ. 10-30W	12V typ. 10W	5V-14V typ. 8W	5V typ. 10W
PCI Express Lanes	2 / 6	4 / 6	2 / 6 (1-5 avail.)	1 / 6	2 / 4 (2 available)
PCI 32bit	–	1 / 1	1 / 1 (needs PCIe)	–	–
USB 2.0 Ports	8 / 8	8 / 8	4 / 8	4 / 8	8 / 8
USB Client Port	0 / 1	–	–	0 / 1	–
LAN Port	0 / 1	1 / 1	1 / 1 (needs PCIe)	1 / 1	1 / 1 (PCIe)
HD Audio AC97	1 / 1	1 / 1	0 / 1	0 / 1	1 / 1
PATA	0 / 1	1 / 1	1 / 1	0 / 0	–
SATA	0 / 4	2 / 4	2 / 4 (needs PCIe)	0 / 4	2 / 2 (PCIe)
Analog VGA	–	1 / 1	0 / 1, not avail.	0 / 1	–
LVDS Ports	0 / 1	1 / 1	0 / 1	0 / 1	2 / 2
SDVO	1 / 1	0 / 1	1 / 1	–	1 / 1
PEG x16	–	1 / 1	1 / 1, not avail.	–	–
TV Output	–	1 / 1	1 / 1, not avail.	0 / 1	–
LPC, SMB	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
SDIO/MMC Port	0 / 1	–	shared with GP	shared with GP	–
Express Card Support	0 / 1	1 / 2	1 / 2, not avail.	1 / 2	–
CAN-Bus	0 / 1	–	–	–	–
Connector	220pin	2x 220pin	2x 220pin	1x 220pin	230pin

8. INDEX